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Two-Terminal Nonvolatile Memories Based on Single-Walled Carbon Nanotubes

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ABSTRACT Reproducible current hysteresis is observed in semiconducting single-walled carbon nanotubes (SWCNTs) measured in a two-terminal configuration without a gate electrode. On the basis of this hysteresis, a two-terminal nonvolatile memory is realized by applying voltage pulses of opposite polarities across the SWCNT. Charge trapping at the SWCNT/SiO_2 interface is proposed to account for the observed phenomena; this explanation is supported by the direct correlation between the switching behaviors and SWCNT carrier types. In particular, a change in dominant carrier type induced by adsorbates in air leads to the direct transition of hysteresis evolution in the same device, providing further evidence for the proposed mechanism.

KEYWORDS: nanotube · resistive switching · memory · charge · two-terminal

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Various nanowires,[1,2] owing to their quasi-one-dimensional structures, have been studied to show new and enhanced functions, and they serve as proofs-of-concept for device designs that are built from the bottom-up. In particular, single-walled carbon nanotubes (SWCNTs) are of great interest for their extremely small diameters and good electronic properties.[3] Through various efforts such as contact and structure optimizations,[4−6] SWCNT-based field effect transistors (FETs) have been demonstrated to rival the state-of-art silicon FETs in some aspects of their functions.[7−9] One proposed application is SWCNT-FET-based nonvolatile memory,[5,6,10−14] in which memory/conduction states are modulated and retained by trapped charges controlled through a third (gate) electrode. In the pursuit of high-density memories, conventional device scaling is expected to reach a limit in the near future.[15] Two-terminal memories based on resistive switching materials[16] may sidestep this problem through equivalent scaling.[15] With the diameter of a SWCNT comparable to that of a single filament in resistive switching materials,[17] a SWCNT-based two-terminal memory could combine the merits of simpler structure and small dimensions.

Here we report reproducible current hysteresis in semiconducting SWCNTs in a two-terminal configuration without the third gate electrode. Based on hysteresis, bistable conduction states between low conductance and high conductance are achieved by applying voltage pulses of opposite polarities across the SWCNT, rendering a two-terminal nonvolatile memory device. Charge trapping at the SWCNT/SiO_2 interface is proposed to account for the observed phenomena. This proposed mechanism is supported by the direct link between the switching behaviors and dominant charge carrier types (electrons or holes) in the SWCNTs. In particular, a transition in dominant carrier type induced by adsorption in air leads to the direct transition of hysteresis evolution in the same device, providing further evidence for the proposed mechanism.

RESULTS AND DISCUSSION

A highly doped Si substrate ($\rho = 0.005$ $\Omega \cdot$cm) with a 200 nm thick thermal SiO_2 layer (purchased from Silicon Quest International, Inc.) was used for SWCNT growth. At 975 °C, an ultralow-gas-flow chemical vapor deposition strategy (details can be found in ref 18) was adopted to grow long and sparsely aligned SWCNTs to facilitate device fabrications. The heights of the SWCNTs were determined by an ambient atomic force microscope (AFM) to be ~2 nm. Standard electron beam lithography was used, followed by metal depositions (40 nm thick Pt with a 5 nm thick Ti adhesion layer) and a lift-off process to define the electrodes on top of the SWCNTs. Electrical characterizations were performed using an Agilent 4155C semiconductor parameter analyzer at room temperature

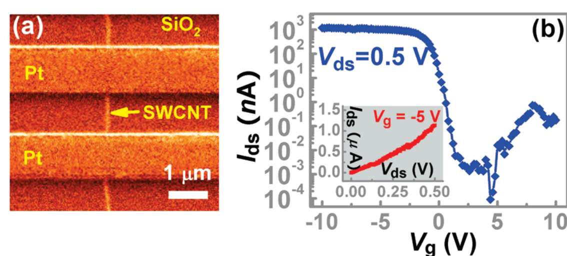

Figure 1. (a) An SEM image of a typical SWCNT device. (b) $I_{ds}-V_g$ curve of the SWCNT device with V_{ds} = 0.5 V (since the current is at the noise level in the depletion region, the current spike at ~5 V is noise-related). Inset: $I_{ds}-V_{ds}$ curve with V_{ds} = −5 V.

under a vacuum of ~10^{-5} Torr (Desert Cryogenics model CPX, Lakeshore Cryotronics, Inc.), unless otherwise specified.

Figure 1a shows a scanning electron microscope (SEM) image of a typical SWCNT device with an electrode−electrode spacing of ~1 μm. During a standard three-terminal measurement using the Si substrate as a back gate, the gate voltage (V_g) and drain current (I_{ds}) relationship exhibits typical p-type behavior (see Figure 1b). The current level in the accumulation region (I_{on}) is close to the reported value using Pd contacts,[9] and the near-linear transport behavior (see inset in Figure 1b) indicates good electrical contacts between the electrodes and the SWCNT.

For two-terminal measurements, the Si substrate with the SWCNT devices was put on a glass substrate with no back-gate electrode attached. Voltage sweeps were applied at one electrode with the other electrode grounded (see schematic in inset in Figure 2a). Figure 2a shows the typical current−voltage ($I_{ds}-V_{ds}$) evolution in the same SWCNT device as shown in Figure 1. For convenience, I_{ds} is displayed in its absolute value $|I_{ds}|$, which also applies to the following figures. For a voltage sweep loop from 0 to +8 V and then back to 0 V (0 → +8 → 0 V, indicated by the arrows on the right side in Figure 2a), the conduction of the SWCNT changes from a low-resistance (ON) state[19] to a high-resistance (OFF) state, producing a current hysteresis. During the subsequent voltage sweep loop in the negative bias voltage region (0 → −8 → 0 V, indicated by the arrows on the left side in Figure 2a), the conduction of SWCNT changes from an OFF state back to an ON state. This hysteretic behavior is reproducible during the subsequent series of voltage sweeps, and can be summarized as follows: a negative V_{ds} (*e.g.*, −8 V) across the SWCNT can "write" the device into an ON state, whereas a positive V_{ds} (*e.g.*, +8 V) can "erase" the device into an OFF state. Consequently, a two-terminal memory device can be realized by applying voltage pulses of −8 or +8 V across the SWCNT to write or erase the memory states. Figure 2b demonstrates a series of memory cycles using voltage pulses of −8, +0.5, and +8 V, as writing, reading (5 times), and erasing operations, respectively. A bistable nondestructive read state

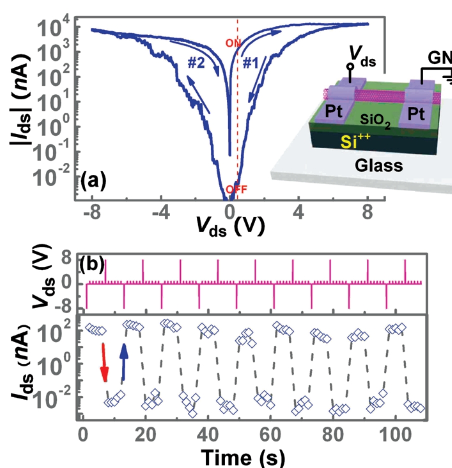

Figure 2. Both panels represent the same p-type SWCNT device tested under vacuum. (a) Two-terminal current−voltage ($I_{ds}-V_{ds}$) evolution in the SWCNT device. The arrows indicate the voltage sweep directions, and numbers indicate the sweep order. The red dashed line indicates an ON state and an OFF state read at +0.5 V. Inset: Schematic of the two-terminal configuration for electrical measurements. (b) (Top panel) A series of programming voltage pulses of −8 and +8 V applied across the device. Between each two neighboring programming voltages, there are five voltage pulses of +0.5 V as reading operations. All the pulse widths used are 300 ms. (Bottom panel) Corresponding memory states (I_{ds}) read out by the +0.5 V pulses shown in the top panel. Note that the I_{ds}, at the programming voltage pulses of either −8 or +8 V, is not shown. The red arrow shows an erasing operation (from ON to OFF) by a +8 V pulse, whereas the blue arrow shows a writing operation (from OFF to ON) by an −8 V pulse.

with an ON−OFF ratio over 10^4 is achieved, which can also been inferred from the current hysteresis loops shown in Figure 2a.

The good electrical contacts between the SWCNT and electrodes (see inset in Figure 1b) indicate that the conductance change does not result from electrical annealing of the contacts,[20] which would be irreversible. Other contact effects such as residual TiO_X switching[21] at the Pt/Ti/SWCNT interface can also be ruled out by the fact that devices with pure Pt electrodes still produce similar hysteresis and switching phenomena. The same amplitudes of voltage pulses used for both writing and erasing operations and the similar local heating due to current in the SWCNT during the two processes indicate that the effect is not due to heat-induced defeat healing[22,23] in the SWCNT. In fact, this kind of self-healing is irreversible in carbon nanotubes (CNTs)[23] or requires very sharp and short pulses (*e.g.*, < 100 ns) for the preparation of an OFF state in the amorphous carbon form.[24] This is in contrast to the reproducibility demonstrated in the present SWCNT device and longer pulses used at the millisecond level. CNT-based two-terminal memory working with a unipolar mechanism was recently demonstrated,[25] in which electrical breakdown in CNTs is needed to produce a gap. The memory effect is attributed to SiO_X switching[25,26] at the gap region with the broken CNT ends merely serving as closely spaced ef-

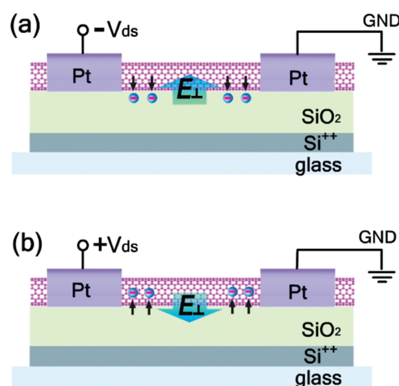

Figure 3. Schematic of charge (electron, represented as blue circle) migration at the SWCNT/SiO_2 interface when a (a) negative or (b) positive V_{ds} is applied across the SWCNT. The big blue arrows in the middle indicate the directions toward which the $E_\perp$ is pointing, and the small black arrows indicate the directions of electron migration.

fective electrodes. Here the switching in the SWCNT device works in a bipolar way (see Figure 2b) with no electrical breakdown involved.

We propose that charge (electron) migration at the SWCNT/SiO_2 interface is responsible for the observed hysteretic and switching behaviors. When a V_{ds} is applied across the device, an electric field component perpendicular to the SWCNT surface ($E_\perp$) is expected. A negative V_{ds} produces an $E_\perp$ pointing into the SWCNT (see illustration in Figure 3a), dragging free electrons from the SWCNT to the SWCNT/SiO_2 interface. The electrons are then trapped there and serve as an effective negative gating, turning the p-type SWCNT into an ON state. Similarly, a positive V_{ds} produces an $E_\perp$ pointing out of the SWCNT (see illustration in Figure 3b), which pulls the electrons from the SWCNT/SiO_2 interface. The electron depleted SWCNT/SiO_2 interface then works as an effective positive gating, turning the p-type SWCNT to an OFF state. This charge-trapping model is supported by the polarities of writing/erasing operations shown in Figure 2b (indicated by blue and red arrows, respectively), in which a negative/positive V_{ds} pulse indeed produces the corresponding ON/OFF state as proposed.

The proposed mechanism is supported by the switching behaviors in an n-type SWCNT device (Figure 4). Because of the opposite gating effect between n-type and p-type SWCNTs, it is straightforward to expect that a set of negative/positive voltages which writes/erases the p-type SWCNT into corresponding ON/OFF states will now do the opposite to erase/write the n-type SWCNT into OFF/ON states, respectively. Figure 4a shows the evolution of current hysteresis in an n-type SWCNT. For a positive voltage sweep loop (0 → +12 → 0 V, see right side in Figure 4a), the conduction of the SWCNT changes from an OFF state into an ON state, as opposed to that from ON to OFF in the p-type SWCNT (compare to right side in Figure 2a). Similarly, the subsequent negative voltage sweep loop (0 → −12 → 0 V, see left side in Figure 4a) features the opposite trend, too. The conduction of the SWCNT changes from an ON state to OFF state, as opposed to that from OFF to ON in the p-type SWCNT (see left side in Figure 2a). Accordingly, this opposite hysteresis evolution compared to that in the p-type SWCNT is also reflected in the memory cycles (see middle panel in Figure 4d), in which a positive programming V_{ds} pulse now becomes a writing operation, whereas a negative programming V_{ds} pulse becomes an erasing one.

The transition of the switching behaviors in the same device, as a result of SWCNT n- to p-type change, discounts individual device variations from consideration and provides added evidence for the proposed mechanism. The electrical measurements of the device shown in Figure 4a were done in vacuum (~10^{-5} Torr) after pumping for 3 h. Besides the dominant n-type transport behavior, there is also a visible p-type tail in the negative gate voltage region (see red curve in Figure 4b), showing ambipolar[27] trait. Exposing the device in air for 24 h leads to the suppression of the n-type

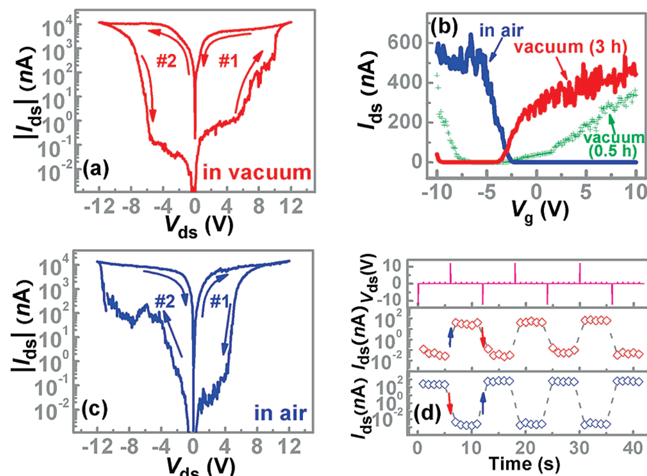

Figure 4. All panels represent the same SWCNT device exposed to varying environments and measurement sequences. Note that a p-type SWCNT can change to an n-type dominant one through adsorbate removal by continued evacuation.[28] (a) Two-terminal $I_{ds}-V_{ds}$ evolution in a second SWCNT device in vacuum (pumping for 3 h). The arrows indicate the voltage sweep directions and the numbers indicate the sweep orders. (b) $I_{ds}-V_g$ (SWCNT-type) transition in the same device. The red curve was measured in a vacuum environment (pumping for 3 h), showing dominant n-type behavior (corresponding to panel a). The blue curve was measured in an ambient environment after 24 h exposure to air, showing p-type behavior (corresponding to panel c). The green curve shows intermediate ambipolar behavior in vacuum (pumping for 0.5 h). (c) $I_{ds}-V_{ds}$ evolution of the device in ambient environment after 24 h of exposure to air. (d) (Top panel) A series of programming voltage pulses of −12 and +12 V. Between each two neighboring programming voltages, there are five voltage pulses of + 0.5 V as reading operations. The corresponding memory states (I_{ds}) read out by the +0.5 V pulses are shown in the middle panel (in vacuum, pumping for 3 h) and the bottom panel (in air). The blue and red arrows show writing and erasing operations, respectively.

transport and the enhancement of p-type transport (see blue curve in Figure 4b), resulting in a SWCNT-type transition into p-type behavior due to oxygen adsorption.[28] During the subsequent measurements in ambient environment using the two-terminal configuration as described before, the evolution of the current hysteresis (see Figure 4c) acquires a reverse trend compared to that observed in vacuum (see Figure 4a), becoming that of a typical p-type device as described previously in Figure 2a. This SWCNT-type transition induced reversal in hysteresis evolution is again reflected in the corresponding memory cycles, in which a negative/positive V_{ds} pulse that previously erases/writes the device into OFF/ON state in vacuum (see middle panel in Figure 4d) now writes/erases the device into ON/OFF in air (see bottom panel in Figure 4d).

Not surprisingly, current hysteresis was not observed in metallic SWCNTs because of their intrinsic insensitivity to gating (see S1 in Supporting Information). This distinguishes the conductance change in our SWCNT devices from phase transition behaviors observed in metallic SWCNTs by electron irradiation[29,30] or by molecular assembly.[31] No phase transition, for example, between semiconducting and metallic states, was observed in our SWCNT devices. The switching SWCNTs retain their semiconducting properties during different memory states, which was confirmed by standard three-terminal measurements using the Si substrate as a back gate.

The reproducibility of the current hysteresis was further tested by memory cycling in vacuum. The SWCNT device shows no obvious degradation after 1000 continuous cycles (see Figure 5a), indicating good memory durability during programming. The stored conduction states show a nonvolatile property with the retention time dependent on the environment. The conductance of an OFF state increases ~3 orders of magnitude after ~5 h in an ambient environment (see red curve in Figure 5b), whereas it only increases ~1 order of magnitude after 15 h in vacuum (see green dashed curve in Figure 5b).

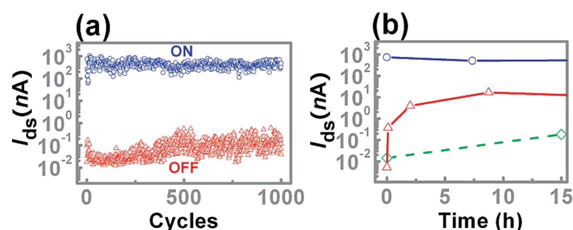

Figure 5. (a) There are 10^3 memory cycles in a SWCNT device using −12, +12, and +0.5 V as writing, erasing, and reading operations, respectively. (b) Retention of memory states in ambient environment for ON (blue curve) and OFF (red curve) states. The dashed green curve shows the decay of the OFF state in vacuum.

This is consistent with the charge-trapping mechanism since atmospheric water has been reported to assist in the discharging process at the SWCNT/SiO_2 interface.[32,33] Meanwhile, the conductance of an ON state only shows a small decrease after a 7 h air exposure (see blue curve in Figure 5b), and retains a similar value afterward (*e.g.*, after 30 d in air). The retention time in the ON state, exceeding the charge storage stability of the reported 14 days,[6,10] indicates that the pristine conduction state of the SWCNT is close to an ON state, which may be due to a constant gate threshold voltage shift commonly observed in SWCNTs. This supplements the proposed mechanism such that, instead of having to charge/discharge the SWCNT/SiO_2 interface along the entire SWCNT, local charge trapping can now pinch off the device, while discharging this local region can bring the device back to the ON state.

CONCLUSIONS

In summary, current hysteresis is observed in semiconducting SWCNTs. A two-terminal nonvolatile memory is demonstrated on the basis of the hysteresis. The direct link between the hysteretic/switching behaviors and SWCNT types supports a mechanism in which charge trapping at the SWCNT/SiO_2 interface is the most likely cause. Our study gives rise to the possibility of constructing SWCNT-based memories with structures that are simpler than previous embodiments.

EXPERIMENTAL SECTION

Highly doped Si substrates (ρ = 0.005 Ω·cm) with a 200 nm thick thermal SiO_2 layer were purchased from Silicon Quest International, Inc. Fe−Mo nanoparticles having diameters of ~2 nm were then used as catalysts for aligned SWCNT growth. The growth was carried out at 975 °C for 10−15 min, with a methane (CH_4) flow rate of 2 sccm and hydrogen (H_2) flow rate of 4 sccm (more details can be found in ref 18). Electrical contacts were patterned using standard electron beam lithography on a JSM-6500F SEM system (JEOL Ftd.). Pt/Ti electrodes were then deposited using a CrC-150 Sputtering System (TORR International Inc.) with a base pressure of 5.0 × 10^{-5} Torr. The diameters of the SWNTs were determined by an ambient AFM system. Electrical characterizations were performed using an Agilent 4155C Semiconductor Parameter Analyzer.

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Supporting Information Available: Electrical testing data. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Lu, W.; Lieber, C. M. Nanoelectronics From the Bottom Up. *Nat. Mater.* **2007**, *8*, 841–850.

2. Li, Y.; Qian, F.; Xiang, J.; Lieber, C. M. Nanowire Electronic and Optoelectronic Devices. *Mater. Today* **2006**, *9*, 18–27.
3. Cao, Q.; Rogers, J. A. Ultrathin Films of Single-Walled Carbon Nanotubes for Electronics and Sensors: A Review of Fundamental and Applied Aspects. *Adv. Mater.* **2009**, *21*, 29–53.
4. Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. Ballistic Carbon Nanotube Field-Effect Transistors. *Nature* **2003**, *424*, 654–657.
5. Fu, W.; Xu, Z.; Bai, X.; Gu, C.; Wang, E. Intrinsic Memory Function of Carbon Nanotube-Based Ferroelectric Field-Effect Transistor. *Nano Lett.* **2009**, *9*, 921–925.
6. Rinkio, M.; Johansson, A.; Paraoanu, G. S.; Torma, P. High-Speed Memory From Carbon Nanotube Field-Effect Transistors with High-Kappa Gate Dielectric. *Nano Lett.* **2009**, *9*, 643–647.
7. Zhang, Z.; Wang, S.; Ding, L.; Liang, X.; Pei, T.; Shen, J.; Xu, H.; Chen, Q.; Cui, R.; Li, Y.; Peng, L.-M. Self-Aligned Ballistic n-Type Single-Walled Carbon Nanotube Field-Effect Transistors with Adjustable Threshold Voltage. *Nano Lett.* **2008**, *8*, 3696–3701.
8. Weitz, R. T.; Zschieschang, U.; Forment-Aliaga, A.; Kalblein, D.; Burghard, M.; Kern, K.; Klauk, H. Highly Reliable Carbon Nanotube Transistors with Patterned Gates and Molecular Gate Dielectric. *Nano Lett.* **2009**, *9*, 1335–1340.
9. Chen, Z.; Appenzeller, J.; Knoch, J.; Lin, Y.-M.; Avouris, P. The Role of Metal-Nanotube Contact in the Performance of Carbon Nanotube Field-Effect Transistors. *Nano Lett.* **2005**, *5*, 1497–1502.
10. Cui, J. B.; Sordan, R.; Burghard, M.; Kern, K. Carbon Nanotube Memory Devices of High Charge Storage Stability. *Appl. Phys. Lett.* **2002**, *81*, 3260–3262.
11. Radosavljevic, M.; Freitag, M.; Thadani, K. V.; Johnson, A. T. Nonvolatile Molecular Memory Elements Based on Ambipolar Nanotube Field Effect Transistors. *Nano Lett.* **2002**, *2*, 761–764.
12. Fuhrer, M. S.; Kim, B. M.; Durkop, T.; Brintlinger, T. High-Mobility Nanotube Transistor Memory. *Nano Lett.* **2002**, *2*, 755–759.
13. Ganguly, U.; Kan, E. C.; Zhang, Y. Carbon Nanotube-Based Nonvolatile Memory with Charge Storage in Metal Nanocrystals. *Appl. Phys. Lett.* **2005**, *87*, 043108.
14. Choi, W. B.; Chae, S.; Bae, E.; Lee, J.-W. Carbon-Nanotube-Based Nonvolatile Memory with Oxide-Nitride-Oxide Film and Nanoscale Channel. *Appl. Phys. Lett.* **2003**, *82*, 275–277.
15. Sawa, A. Resistive Switching in Transition Metal Oxides. *Mater. Today* **2008**, *11*, 28–36.
16. Waser, R.; Aono, M. Nanoionics-Based Resistive Switching Memories. *Nat. Mater.* **2007**, *6*, 833–840.
17. Szot, K.; Speier, W.; Bihlmayer, G.; Waser, R. Switching the Electrical Resistance of Individual Dislocations in Single-Crystalline $SrTiO_3$. *Nat. Mater.* **2006**, *5*, 312–320.
18. Jin, Z.; Chu, H.; Wang, J.; Hong, J.; Tan, W.; Li, Y. Ultralow Feeding Gas Flow Guiding Growth of Large-Scale Horizontally Aligned Single-Walled Carbon Nanotube Arrays. *Nano Lett.* **2007**, *7*, 2073–2079.
19. For the convenience of comparison and the reproducibility of the hysteresis, a voltage sweep in the negative bias region was performed prior to the first voltage sweep shown in the positive bias region. The same rule applies to all the following hysteretic curves. According to the hysteresis evolutions described here and hereinafter, it initializes the device into an ON state for a p-type SWCNT and an OFF state for an n-type SWCNT.
20. Wang, H.; Wang, X.; Li, X.; Dai, H. Chemical Self-Assembly of Graphene Sheets. *Nano Res.* **2009**, *2*, 336–342.
21. Yang, J. J.; Pickett, M. D.; Li, X.; Ohlberg, D. A. A.; Stewart, D. R.; Williams, R. S. Memristive Switching Mechanism for Metal/Oxide/Metal Nanodevices. *Nat. Nanotechnol.* **2008**, *3*, 429–433.
22. Suekane, O.; Nagataki, A.; Nakayama, Y. Current-Induced Curing of Defective Carbon Nanotubes. *Appl. Phys. Lett.* **2006**, *89*, 183110.
23. Huang, J. Y.; Shen, S.; Ren, Z. F.; Chen, G.; Dresselhaus, M. S. Real-Time Observation of Tubule Formation from Amorphous Carbon Nanowires under High-Bias Joule Heating. *Nano Lett.* **2006**, *6*, 1699–1705.
24. Kreupl, F.; Bruchhaus, R.; Majewski, P.; Philipp, J. B.; Symanczyk, R.; Happ, T.; Arndt, C.; Vogt, M.; Zimmermann, R.; Buerke, A.; *et al*. Carbon-Based Resistive Memory. *Tech. Dig.—Int. Electron Device Meet.* **2008**, p. 521–524.
25. Yao, J.; Zhong, L.; Zhang, Z.; He, T.; Jin, Z.; Wheeler, P. J.; Natelson, D.; Tour, J. M. Resistive Switching in Nanogap Systems on SiO_2 Substrates. Small, published online September 28, 2009. http://dx.doi.org/10.1002/smll.200901100.
26. Yao, J.; Zhong, L.; Natelson, D.; Tour, J. M. Etching-Dependent Reproducible Memory Switching in Vertical SiO_2 Structures. *Appl. Phys. Lett.* **2008**, *93*, 253101.
27. Martel, R.; Derycke, V.; Lavoie, C.; Appenzeller, J.; Chan, K. K.; Tersoff, J.; Avouris, P. Ambipolar Electrical Transport in Semiconducting Single-Wall Carbon Nanotubes. *Phys. Rev. Lett.* **2001**, *87*, 256805.
28. Kang, D.; Park, N.; Hyun, J.; Bae, E.; Ko, J.; Kim, J.; Park, W. Adsorption-Induced Conversion of The Carbon Nanotube Field Effect Transistor from Ambipolar to Unipolar Behavior. *Appl. Phys. Lett.* **2005**, *86*, 093105.
29. Marquardt, C. W.; Dehm, S.; Vijayaraghavan, A.; Blatt, S.; Hennrich, F.; Krupke, R. Reversible Metal-Insulator Transitions in Metallic Single-Walled Carbon Nanotubes. *Nano Lett.* **2008**, *8*, 2767–2772.
30. Vijayaraghavan, A.; Kanzaki, K.; Suzuki, S.; Kobayashi, Y.; Inokawa, H.; Ono, Y.; Kar, S.; Ajayan, P. M. Metal-Semiconductor Transition in Single-Walled Carbon Nanotubes Induced by Low-Energy Electron Irradiation. *Nano Lett.* **2005**, *5*, 1575–1579.
31. Cha, M.; Jung, S.; Cha, M.-H.; Kim, G.; Ihm, J.; Lee, J. Reversible Metal-Semiconductor Transition of ssDNA-Decorated Single-Walled Carbon Nanotubes. *Nano Lett.* **2009**, *9*, 1345–1349.
32. Ong, H. G.; Cheah, J. W.; Chen, L.; TangTang, H.; Xu, Y.; Li, B.; Zhang, H.; Li, L.-J.; Wang, J. Charge Injection at Carbon Nanotube-SiO_2 Interface. *Appl. Phys. Lett.* **2008**, *93*, 093509.
33. Lee, J. S.; Ryu, S.; Yoo, K.; Choi, I. S.; Yun, W. S.; Kim, J. Origin of Gate Hysteresis in Carbon Nanotube Field-Effect Transistors. *J. Phys. Chem. Lett. C* **2007**, *111*, 12504–12507.